CLAIMS

What is claimed:

1. A microelectronic assembly, comprising:

a die substrate;

an integrated circuit formed on the die substrate, the die substrate and integrated circuit jointly forming a die; and

a plurality of thermoelectric elements formed on the die so as to pump heat away from the die when current flows through the thermoelectric elements.

2. The microelectronic assembly of claim 1, wherein the thermoelectric elements are formed on a side of the die, with the integrated circuit between the die substrate and the thermoelectric elements.

3. The microelectronic assembly of claim 2, wherein the integrated circuit includes a power plane connected to the thermoelectric components, such that power is provided through the thermoelectric components to the power plane.

4. The microelectronic assembly of claim 3, further comprising a power conductive interconnection element formed on each thermoelectric component.

5. The microelectronic assembly of claim 4, further comprising a plurality of ground and signal conductive interconnection elements having contact surfaces in a

plane of contact surfaces of the power conductive interconnection elements.

6. The microelectronic assembly of claim 5, further comprising a carrier substrate and a plurality of carrier substrate lands on the carrier substrate, each conductive interconnection element being located against a respective carrier substrate land.

7. The microelectronic assembly of claim 2, further comprising a dielectric material surrounding the thermoelectric elements.

8. The microelectronic assembly of claim 2, wherein the thermoelectric components are in pairs, each pair including a respective thermoelectric component that is p-doped and a respective thermoelectric component that is n-doped, further comprising a plurality of link elements formed on the die, each link element interconnecting two interconnection elements of a respective pair.

9. The microelectronic assembly of claim 1, wherein the thermoelectric elements are formed on a side of the die, with the integrated circuit between the die substrate and the thermoelectric elements, further comprising a dielectric material surrounding the thermoelectric elements, and wherein the integrated circuit includes a power plane connected to the thermoelectric components such that power is provided through the thermoelectric components to the power plane.

10. The microelectronic assembly of claim 8, further comprising a carrier substrate and a plurality of carrier substrate lands on the carrier substrate, each conductive interconnection element being located against a respective carrier substrate land.

11. The microelectronic assembly of claim 1, wherein the thermoelectric elements are formed on a side of the die, with the die substrate between the integrated circuit and the thermoelectric elements.

12. The microelectronic assembly of claim 11, further comprising a dielectric material surrounding the thermoelectric elements.

13. The microelectronic assembly of claim 11, wherein the thermoelectric components are in pairs, each pair including a respective thermoelectric component that is p-doped and a respective thermoelectric component that is n-doped, further comprising a plurality of link elements formed on the die, each link element interconnecting two interconnection elements of a respective pair.

14. The microelectronic assembly of claim 11, further comprising a carrier substrate, the die being mounted to the carrier substrate and the thermoelectric elements being electrically connected to the carrier substrate to receive power from the carrier substrate.

15. The microelectronic assembly of claim 14, further comprising a plurality of carrier substrate lands on the carrier substrate, a plurality of thermoelectric lands connected to the thermoelectric elements, and a plurality of wirebonding wires, each having one portion attached to a respective carrier substrate land and another portion attached to a respective thermoelectric land.

16. The microelectronic assembly of claim 15, wherein the thermoelectric lands are formed on the die substrate.

17. The microelectronic assembly of claim 16, further comprising a plurality of conductive interconnection elements attached to the die on a side thereof with the integrated circuit between the conductive interconnection elements and the die substrate, each conductive interconnection element being in contact with a respective one of the carrier substrate lands.

18. The microelectronic assembly of claim 11, further comprising a plurality of conductive interconnection elements attached to the die on a side thereof with the integrated circuit between the conductive interconnection elements and the die substrate, each conductive interconnection element being in contact with a respective one of the carrier substrate lands.

19. The microelectronic assembly of claim 18, further comprising a plurality of

thermoelectric vias in the die, a first plurality of the conductive interconnection elements connecting the integrated circuit with a first plurality of the carrier substrate lands and a second plurality of the conductive interconnection elements being connected through the thermoelectric vias to the thermoelectric elements.

20. The microelectronic assembly of claim 19, wherein at least one of the thermoelectric elements is aligned with one of the thermoelectric vias and one of the conductive interconnections elements.

21. The microelectronic assembly of claim 1, further comprising a plurality of die lands on the die, a plurality of first diffusion barrier layers, each on a respective die land, each thermoelectric element being formed on a respective diffusion barrier layer.

22. The microelectronic assembly of claim 21, further comprising at least one second diffusion barrier layer on at least one of the thermoelectric elements, with the respective thermoelectric element between a respective one of the first diffusion barrier layers and the second diffusion barrier layer.

23. The microelectronic assembly of claim 21, wherein the thermoelectric elements are formed on a side of the die, with the integrated circuit between the die substrate and the thermoelectric elements.

24. The microelectronic assembly of claim 22, wherein the thermoelectric elements are formed on a side of the die, with the die substrate between the integrated circuit and the thermoelectric elements.

25. The microelectronic assembly of claim 24, further comprising a carrier substrate, the die being mounted to the carrier substrate and the thermoelectric elements being electrically connected to the carrier substrate to receive power from the carrier substrate.

26. The microelectronic assembly of claim 1, further comprising a thermally conductive plate thermally coupled to the thermoelectric elements, with the thermoelectric elements between the die and the thermally conductive plate.

27. The microelectronic assembly of claim 26, further comprising a plurality of fins extending from the thermally conductive plate from which heat, conducting from the thermally conductive plate, convects to surrounding air.

28. A method of making a microelectronic assembly, comprising:

forming at least one microelectronic circuit on a first supporting substrate;

forming a plurality of thermoelectric elements on the first supporting substrate, the thermoelectric elements pumping heat away from the microelectronic

circuit when the microelectronic circuit is operated and current flows through the thermoelectric elements.

29. The method of claim 28, wherein the thermoelectric elements are formed after the microelectronic circuit is formed.

30. The method of claim 28, wherein the thermoelectric elements are formed on a side of the die, with the integrated circuit between the die substrate and the thermoelectric elements.

31. The method of claim 30, further comprising forming a power conductive interconnection element on each thermoelectric component.

32. The method of claim 31, further comprising forming a plurality of ground and signal conductive interconnection elements, having contact surfaces in a plane of contact surfaces of the power conductive interconnection elements.

33. The method of claim 32, further comprising locating the conductive interconnection elements against respective lands of a carrier substrate.

34. The method of claim 28, further comprising forming a dielectric material forming a first plurality of openings in the dielectric material, forming

thermoelectric elements of a first conductivity type in the first plurality of openings, subsequently forming a second plurality of openings in the dielectric material, forming thermoelectric elements of a second conductivity type, opposite to the first conductivity type, in the second plurality of openings, and electrically interconnecting pairs of the thermoelectric elements, each pair having one thermoelectric element of the first conductivity type and one thermoelectric element of the second conductivity type.

35. The method of claim 28, further comprising forming the thermoelectric elements on a second supporting substrate, and subsequently connecting the thermoelectric elements to the first supporting substrate.

36. The method of claim 35, wherein the first and second substrates form a combination wafer which is singulated into dies by at least severing one of the supporting substrates.

37. The method of claim 36, wherein the first and second supporting substrates are severed to singulate the combination wafer.

38. A method of making a microelectronic assembly, comprising:

forming at least one microelectronic circuit on a first supporting substrate;

forming thermoelectric elements on a second supporting substrate; and

subsequently connecting the thermoelectric elements to the first supporting substrate.

39. The method of claim 38, wherein the first and second substrates form a combination wafer which is singulated into dies by at least severing one of the supporting substrates.

40. The method of claim 39, wherein the first and second supporting substrates are severed to singulate the combination wafer.